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KLARQUIST SPARKMAN, LLP
121 S.W. SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,143	BOLCATO ET AL.	
	Examiner	Art Unit	
	JASON PROCTOR	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response submitted on 23 April 2010 has amended claims 1, 8-11, 13, 15, 16, 20, 21, and 23. Claims 1-23 are pending in this application.

Claims 1-23 are rejected.

This Office Action includes new grounds of rejection not necessitated by Applicants' amendments. Accordingly, this Office Action is a non-final rejection.

Response to Remarks - 35 USC § 101

1. In response to the previous rejection of claim 13 under 35 U.S.C. § 101 as being directed to computer software *per se* and thus describing nonstatutory subject matter, Applicants argue primarily that:

> Independent claim 13 has been amended to recite "An analog or RF simulator of a computer for simulating a circuit..." and independent claim 21 has been amended to recite "using a computer, generating a system of equations..." Thus, claims 13-17 and 21-23 are directed to statutory subject matter and these rejections should be withdrawn.

The Examiner respectfully traverses this argument as follows.

The previous rejection was entered because claim 13 encompasses a claim scope broad enough to include computer software *per se*. Amending the claim's preamble to recite, in effect, computer software "of a computer" fails to address this deficiency. Even with the amended claim language, the claimed "simulator of a computer" comprising "an elaboration engine" and "a simulation kernel" encompasses computer software *per se* and is nonstatutory subject matter. Applicants' argument has been fully considered but has been found unpersuasive. The previous rejection is maintained.

2. In response to the previous rejection of claim 21 under 35 U.S.C. § 101 as being directed to nonstatutory method, Applicants argue primarily that:

> Independent claim 13 has been amended to recite "An analog or RF simulator of a computer for simulating a circuit..." and independent claim 21 has been amended to recite "using a computer, generating a system of equations..." Thus, claims 13-17 and 21-23 are directed to statutory subject matter and these rejections should be withdrawn.

The Examiner has fully considered this argument and finds it persuasive. The previous rejection of claims 21-23 under 35 U.S.C. § 101 is withdrawn.

Response to Remarks - 35 USC § 112, first paragraph

3. In response to the previous rejection of claims 18-20 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement in relation to the several "means for" limitations, Applicants have responded by pointed out the specific instances of support for the claimed features in the specification (See Applicants' remarks, pages 7 to 8 of 13). In response to the remarks, the previous rejection of claims 18-20 under 35 U.S.C. § 112, first paragraph, is withdrawn.

Response to Remarks - 35 USC § 112, first paragraph

4. In response to Applicants' remarks and amendments to the claims, the previous rejections of claims 8, 9, 10, 15, 16, 18-20, and 23 under 35 U.S.C. § 112, second paragraph, are withdrawn.

Response to Remarks - 35 USC § 102

5. In response to the previous rejection of claims 1-3, 7, and 10 under 35 U.S.C. § 102(e) as being anticipated by Teene, Applicants argue primarily that:

> Teene mentions a "functional simulation" that "generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation" (3:60-63) and a "full instance resistance and capacitance extraction" in which "a layout extraction is performed to determine the values of all the parasitic capacitances and resistances" (4:10-19). Teene clearly does not teach or even suggest using two different circuit descriptions in a single simulation, as required by amended claim 1.

The Examiner has fully considered this argument and finds it persuasive. Accordingly, the previous rejection has been withdrawn. New grounds of rejection are entered below.

Response to Remarks - 35 USC § 103

6. The previous rejections under 35 U.S.C. § 103(a) all relied in part upon the Teene reference. Applicants' remarks have distinguished the claimed invention over the teachings of the Teene reference. Accordingly, those rejections which relied at least in part on the Teene reference have been withdrawn. New grounds of rejections are entered below.

Regarding the secondary references Gullapalli and McDonald, Applicants' remarks allege that these references do not cure the deficiencies of Teene or fail to teach certain claimed limitations resulting from the deficiencies of Teene (see, in particular, Applicants' Remarks, page 12 of 13, alleging that Gullapalli does not teach a system of equations that uses two different circuit descriptions). These arguments have been fully considered, but are regarded as moot in view of the new grounds of rejection set forth below.

Claim Interpretation - 35 USC § 101

7. Claims 1-12 define a method of simulating a circuit using an analog or RF simulator. In the context of the disclosure, this method is interpreted as being inherently tied to a computing device. These claims are therefore found to meet the requirements of 35 U.S.C. § 101 for statutory subject matter.

8. Claims 18-21 define a simulator for simulating a circuit. In the context of the disclosure, this simulator is interpreted as being inherently tied to a computer device. However, these claims recite "means for" limitations that are not adequately described by the disclosure, as explained below. These claims appear to meet the requirements of 35 U.S.C. § 101 for statutory subject matter because these claims appear to define an apparatus.

If Applicants find this interpretation improper or undesirable, clarification or amendment of the claim language is required.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 13-17 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claim 13 defines "an analog or RF simulator for simulating a circuit" comprising "an elaboration engine" and "a simulation kernel". In the context of the specification, the claimed simulator is computer software per se. Computer software per se is none of the categories of

invention set forth in 35 U.S.C. § 101. Claim 13 is therefore directed to non-statutory subject matter. None of dependent claims 14-17 overcome this deficiency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

10. Claims 1-5, 7, and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,424,959 to Bennett, III et al. ("Bennett") in view of US Patent No. 5,960,181 to Sanadidi et al. ("Sanadidi").

Regarding claim 1, Bennett teaches a method of simulating a circuit using an analog or RF simulator, comprising:

defining two circuit descriptions to be used during the simulation, a first circuit description used for accuracy of the simulation ["*Second, the exact physical location of each component and wire affects the overall behavior of all circuits to some extent. Physical location is important because electrical components subtly interact with one another based on their physical location. These interactions, called parasitic effects, are generally small and may not be important to the performance of simple circuits operating in non-challenging regimes. However, parasitic effects may crucially affect the performance of a circuit operating, say, at radio frequencies (RF). For many operating regimes, it is impossible to design an acceptable and practical circuit without considering parasitic effects. If the physical location of components and wires is considered relevant to determining the behavior of the circuit, the user may pass the netlist (with the added information about the physical location of the components) to a commercially available simulator that considers such information as part of its simulation. For example, Hewlett-Packard of Palo Alto, Calif. markets a simulator for radio frequency (RF) circuits composed of capacitors, inductors, and resistors that considers the physical location of the components and wires in determining the circuit's overall behavior. Alternatively, there is a commercially available tool (one of which is called MAGIC from the University of California at*

Berkeley and one of which is available from Advanced Microelectronics of Ridgeland, Mass. that takes, as its inputs, a netlist (with information about the physical location of the components) and that produces a new (and expanded) netlist that contains additional components that represent the parasitic effects of each of the original components. The expanded netlist may then be supplied as input to a circuit simulator such as SPICE. In both approaches, the result is a simulation of the circuit that conside3rs the effect of the physical location of the circuit's components and wires." (Bennett, column 21, line 52 - column 22, line 19)]

and a second circuit simulation description, different from the first circuit description, used for increasing the speed of the simulation [*"First, placement and routing are themselves difficult tasks in the process of designing electrical circuits. The user may use the automatically created information about exact physical location of each component (i.e., the placement of components) on the printed circuit board, silicon wafer, or other substrate and the exact physical location of each connecting wire between circuit's components (i.e., the routing of the wires) on the printed circuit board, silicon wafer, or other substrate for the limited (but important) purpose of automatically generating an acceptable placement and routing (layout) of the components and wires. If the user is using the automatically created information for the limited purpose of generating an acceptable placement and routing (layout) of the circuit, then the netlist may be passed, in one embodiment, to a circuit simulator (such as SPICE) in order to determine the circuit's behavior without regard to the physical location of the circuit's components and wires."* (Bennett, column 21, lines 35-52)]; and

simulating the circuit using ***either*** the first and second circuit descriptions to generate a single simulation result (Bennett, column 21, line 35 - column 22, line 19).

Bennett does not expressly teach simulating the circuit with ***both*** the first and second circuit descriptions to generate a single simulation result.

Sanadidi teaches a simulation method including a strategy of "aggregation" wherein a component is modeled by a plurality of different simulation models, ranging from highly detailed to simple [*"Aggregation techniques have previously been successfully used in reducing the computational complexity of large analytic models. Under certain assumptions, details of a system's state can be aggregated and represented by a much smaller state space. As an example, one might replace a detailed model of a disk with a simple delay distribution. This is an approximation and it is necessary to verify that the results will be within acceptable accuracy. In a simulation, the benefit of the simpler subsystem model is that there are fewer events to process per unit of simulation time. This DBC Performance Analysis system model is a platform which will be used by many different people for different purposes. Depending on the purpose, the detail required for different subsystems will vary. It is beneficial then, for a user to be able to choose either a detailed subsystem model or a simplified version. An additional advantage of having both a simplified and a detail version of a submodel comes in speeding up the initial transient phase of a simulation run. The implementation should allow switching from simplified to the detailed version at an appropriate point in a run. To accomplish this "plug and play" mode, both detailed and simplified models are generally required to have identical interfaces to the remaining parts of the system model."* (Sanadidi, column 10, lines 6-28)].

Sanadidi further teaches "cloning," a special form of aggregation [*"Cloning is a special form of aggregation. It applies to cases where there are many replicas of a subsystem in a model and where the workload is statistically the same on each subsystem... There are several*

advantages to cloning over traditional aggregation which stem from the availability of statistics gathered at master submodels. As an example, consider the disk subsystem clones described above. The delays that are experienced at the disk subsystem are work-load dependent. In a more traditional implementation of aggregation, the modeler would have to supply some estimate of the disk subsystem delay as a function of workload. In the case of cloning, the workload dependency is resolved automatically." (Sanadidi, column 10, lines 39-67)].

Sanadidi teaches simulating a component using ***both*** the first (accurate) and second (fast) component models to generate a single simulation result [*"The preferred embodiment can be summarized in reference to FIG. 8 as a computer performance modeling system 300. A first submodel 302 simulates system operations of a particular system component (e.g., step processing component 112 of FIG. 2) in minute detail. A second submodel 304 simulates system operations of the same particular system component in simple detail... The performance analysis mechanism 306 includes a switch 308 for switching between the first 302 and the second 304 submodel through processor 310 control during the simulation at a predetermined point in the execution of the s8imulation by the processor 310."* (Sanadidi, column 17, lines 12-35)].

Bennett and Sanadidi are analogous art because both are drawn to simulation of electronic devices.

It would have been obvious to a person of ordinary skill in the art to combine the teachings of Bennett and Sanadidi as expressly motivated by Sanadidi in order to "speed up the initial transient phase of a simulation run" (Sanadidi, column 10, lines 6-28). That is, in order to simulate the operating state of an RF circuit, Bennett teaches using an expanded netlist with

additional parasitic information (Bennett, column 21, line 52 - column 22, line 19). However, Bennett also teaches a faster, simpler non-parasitic netlist for simulating the same circuit description (Bennett, column 21, lines 35-52). Sanadidi teaches the "aggregation" or "cloning" simulation technique that would utilize ***both*** Bennett's parasitic model (i.e., "submodel 302" which simulates in "minute detail") ***and*** the non-parasitic model (i.e., "submodel 304" which simulates "in simple detail"). Sanadidi further teaches switching from one submodel to the other submodel at certain points during the simulation (Sanadidi, column 17, lines 12-35). The ordinary and predictable result of combining these references would be a simulation with a speedy "initial transient phase" using the "non-parasitic netlist" "simple submodel 304" to initialize the simulation of the RF circuit, and then switching to the "parasitic netlist" "minute detail submodel 302" at the appropriate time in order to accurately simulate the performance of the RF circuit during the operating times with which the user is most concerned. This combination would, in effect, allow a simulation to "fast forward" through simulation times that are not of particular interest using the fast, but less accurate submodel, and switch to the slower, but more accurate submodel during the simulation times that are of particular interest.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Bennett and Sanadidi to arrive at the invention specified in claim 1.

Regarding claim 2, Bennett teaches that the first circuit description comprises parasitic information and the second circuit description has the parasitic information removed or substantially reduced (Bennett, column 21, line 35 - column 22, line 19).

Regarding claim 3, Bennett teaches reading a netlist comprising parasitic information or reading a netlist and a separate file containing parasitic information, and wherein the first circuit description comprises all of the elements included in the netlist plus the parasitic information (Bennett, column 21, line 35 - column 22, line 19).

Regarding claim 4, Bennett in view of Sanadidi teaches comprising modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying comprises: analyzing the first circuit to create parasitic information (Bennett, column 21, line 35 - column 22, line 19).

Bennett in view of Sanadidi does not expressly teach analyzing values and functionality of electrical components in the circuit to determine which components are parasitic information; and

removing the parasitic information based on the analysis.

It would have been obvious to a person of ordinary skill in the art to perform a method that follows Bennett's method to produce a second circuit description with parasitic information included, and to remove that parasitic information to return to a previous stage in the method. This could result from a simulation involving the second circuit description including the parasitic information that reveals unacceptable performance or an error in the circuit design. It would then be common sense and common knowledge to a person of ordinary skill in the art to 1) optionally modify the second circuit design to address the problem, remove the parasitic information, and return to a previous step in the design process; or 2) remove the parasitic

information, return to a previous step in the design process, and modify the design at a previous step to address the problem.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to follow the teachings of Bennett in view of Sanadidi, in combination with ordinary knowledge of a person having ordinary skill in the art, to arrive at the invention specified in claim 4.

Regarding claim 5, Bennett in view of Sanadidi renders obvious the steps of modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying comprises:

identifying circuit components marked as parasitic information; and

removing the parasitic information based on the identification.

It would have been obvious to a person of ordinary skill in the art to perform a method that follows Bennett's method to produce a second circuit description with parasitic information included, and to remove that parasitic information to return to a previous stage in the method. This could result from a simulation involving the second circuit description including the parasitic information that reveals unacceptable performance or an error in the circuit design. It would then be common sense and common knowledge to a person of ordinary skill in the art to 1) optionally modify the second circuit design to address the problem, remove the parasitic information, and return to a previous step in the design process; or 2) remove the parasitic information, return to a previous step in the design process, and modify the design at a previous step to address the problem.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to follow the teachings of Bennett in view of Sanadidi, in combination with ordinary knowledge of a person having ordinary skill in the art, to arrive at the invention specified in claim 5.

Regarding claim 7, Bennett teaches forming a first list comprising circuit components without parasitic information [*"netlist"* (Bennett, column 21, lines 24-52)];

forming a second list comprising the parasitic information [*"netlist"* (Bennett, column 21, line 52 - column 22, line 19)];

forming first and second simulation data structures using the first and second lists, respectively (Bennett, column 21, line 35 - column 22, line 19); and

wherein the first circuit description is defined as a combination of the first and second lists, and the second circuit description is defined as only the first list (Bennett, column 21, line 35 - column 22, line 19).

Regarding claim 18, Bennett teaches a simulator for simulating a circuit, comprising:

means for reading a first description of the circuit that comprises a list of components in the circuit, the interconnections between the components, and parasitic information (Bennett, column 21, line 52 - column 22, line 19);

means for generating a second circuit description by removing at least a part of the parasitic information from the first circuit description (Bennett, column 21, lines 35-52); and

means for simulating the circuit using substantially the first circuit description comprising the parasitic information ***or*** the second circuit description with reduced parasitic information (Bennett, column 21, line 35 - column 22, line 19).

Bennett does not expressly teach simulating the circuit using ***both*** the first circuit description comprising the paraisitic information ***and*** the second circuit description with reduced parasitic information.

Sanadidi teaches simulating a component using ***both*** the first (accurate) and second (fast) component models to generate a single simulation result [*"The preferred embodiment can be summarized in reference to FIG. 8 as a computer performance modeling system 300. A first submodel 302 simulates system operations of a particular system component (e.g., step processing component 112 of FIG. 2) in minute detail. A second submodel 304 simulates system operations of the same particular system component in simple detail... The performance analysis mechanism 306 includes a switch 308 for switching between the first 302 and the second 304 submodel through processor 310 control during the simulation at a predetermined point in the execution of the s8imulation by the processor 310."* (Sanadidi, column 17, lines 12-35)].

Bennett and Sanadidi are analogous art because both are drawn to simulation of electronic devices.

It would have been obvious to a person of ordinary skill in the art to combine the teachings of Bennett and Sanadidi as expressly motivated by Sanadidi in order to "speed up the initial transient phase of a simulation run" (Sanadidi, column 10, lines 6-28). That is, in order to simulate the operating state of an RF circuit, Bennett teaches using an expanded netlist with

additional parasitic information (Bennett, column 21, line 52 - column 22, line 19). However, Bennett also teaches a faster, simpler non-parasitic netlist for simulating the same circuit description (Bennett, column 21, lines 35-52). Sanadidi teaches the "aggregation" or "cloning" simulation technique that would utilize ***both*** Bennett's parasitic model (i.e., "submodel 302" which simulates in "minute detail") and the non-parasitic model (i.e., "submodel 304" which simulates "in simple detail"). Sanadidi further teaches switching from one submodel to the other submodel at certain points during the simulation (Sanadidi, column 17, lines 12-35). The ordinary and predictable result of combining these references would be a simulation with a speedy "initial transient phase" using the "non-parasitic netlist" "simple submodel 304" to initialize the simulation of the RF circuit, and then switching to the "parasitic netlist" "minute detail submodel 302" at the appropriate time in order to accurately simulate the performance of the RF circuit during the operating times with which the user is most concerned. This combination would, in effect, allow a simulation to "fast forward" through simulation times that are not of particular interest using the fast, but less accurate submodel, and switch to the slower, but more accurate submodel during the simulation times that are of particular interest.

Further, it would have been obvious to a person of ordinary skill in the art to perform a method that follows Bennett's method to produce a second circuit description with parasitic information included, and to remove that parasitic information to return to a previous stage in the method. This could result from a simulation involving the second circuit description including the parasitic information that reveals unacceptable performance or an error in the circuit design. It would then be common sense and common knowledge to a person of ordinary skill in the art to 1) optionally modify the second circuit design to address the problem, remove the parasitic

information, and return to a previous step in the design process; or 2) remove the parasitic information, return to a previous step in the design process, and modify the design at a previous step to address the problem.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Bennett and Sanadidi to arrive at the invention specified in claim 18.

11. Claims 6, 8, 9, 11, and 19-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bennett in view of Sanadidi as applied to claims 1 and 18 above, further in view of US Pregrant Publication 2004/0083437 to Gullapalli et al. ("Gullapalli").

Regarding claim 6, Gullapalli teaches that simulating comprises solving a system of interrelated equations, wherein a part of the system of equations uses the first circuit description and wherein a part of the system of equations uses the second circuit description [*"In block 14, circuit equations are generated based on the circuit description and models. These circuit equations embody the traditional circuit laws such as Kirchoff's voltage and current laws (KVL and KCL)... The result is a system of nonlinear differential equations that may be represented by: $F(x) = b$"* (Gullapalli, paragraph 0010).

Gullapalli and Bennet in view of Sanadidi are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli with Bennett in view of Sanadidi

because Gullapalli expressly teaches a method that *"provide*[s] *for distortion analysis to measure the second and third order deviation of a circuit response from a desired linear response using only first order transfer functions."* (Gullapalli, paragraph 0008). Therefore, a person of ordinary skill would expect to achieve more accurate simulations by combining Gullapalli's teachings with Bennett in view of Sanadidi, and therefore to have higher confidence that the simulation accurately represents the performance of an analog device under design.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli and Bennett in view of Sanadidi to arrive at the invention specified in claim 6.

Regarding claim 8, Gullapalli teaches evaluating $F(X^i)$, where F is a function and X^i is a value of a variable X for an iteration *i*, using both the first and second simulation data structures for accuracy and performing a factorization of a Jacobian matrix built using only the first simulation data structure for increasing the speed of the simulation [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations, F(x)=b. The iterative method can be described using the following iterative formula:* [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for j=0 (corresponding to the first iteration), the first order response may be determined, as was described in reference to equation 2 above, where x was determined to be* x_1*, such that the resulting equation can be expressed as* $J(x_1)(x_1-x_0)=b-F(x_0)$*. Note that the*

approximation of x determined from equation 5 rapidly converges towards the actual solution of F(x)=b assuming that small signals are sufficiently small." (Gullapalli, paragraphs 0021-0022)].

Regarding claim 9, Gullapalli teaches that simulating comprises solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components and built using the second circuit description, ΔX is a variable to be solved, F is a function, and X^i is a value of a variable X for an iteration *I*; factorizing the matrix J, evaluating $F(X^i)$ using the first circuit description and solving for ΔX [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations, F(x)=b. The iterative method can be described using the following iterative formula:* [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for j=0 (corresponding to the first iteration), the first order response may be determined, as was described in reference to equation 2 above, where x was determined to be* x_1*, such that the resulting equation can be expressed as* $J(x_1)(x_1-x_0)=b-F(x_0)$*. Note that the approximation of x determined from equation 5 rapidly converges towards the actual solution of F(x)=b assuming that small signals are sufficiently small."* (Gullapalli, paragraphs 0021-0022)].

Regarding claim 11, Gullapalli teaches that simulating further comprises factorizing a Jacobian matrix built using the second circuit description for preconditioning a linear iterative solver (Gullapalli, paragraphs 0021-0022).

Regarding claim 19, Gullapalli teaches means for solving a linear system of equations using an iterative solver or a direct solver (Gullapalli, paragraphs 0021-0022, et seq.).

Regarding claim 20, Gullapalli teaches that the means for simulating comprises evaluating $F(X^i)$ using the first circuit description and factorizing a Jacobian matrix J using the second circuit description to solve an equation $J\Delta X = -F(X^i)$ (Gullapalli, paragraphs 0021-0022, et seq.).

12. Claims 13-16 and 21-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bennett in view of Sanadidi, further in view of Gullapalli.

Regarding claim 13, Bennett teaches an analog or RF simulator for simulating a circuit (Bennett, column 21, line 35 - column 22, line 19), comprising:

an elaboration engine that receives one or more lists associated with the circuit comprising a list of components in the circuit, interconnections between the components, and parasitic information and that defines two circuit descriptions, a first circuit description used for accuracy of the simulation and a second circuit description used for speed of the simulation, the first circuit description being different from the second circuit description (Bennett, column 21, line 35 - column 22, line 19).

Sanadidi teaches a simulation system that uses a first submodel ("first circuit description") used for accuracy of the simulation and a second submodel ("second circuit

description") used for speed of the simulation, the first submodel being different from the second submodel (Sanadidi, column 17, lines 12-35).

Gullapalli teaches a simulation kernel coupled to the elaboration engine that comprises at least a direct solver or linear iterative solver to simulate the circuit, wherein the simulation kernel solves a system of equations [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations, F(x)=b. The iterative method can be described using the following iterative formula:* [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for j=0 (corresponding to the first iteration), the first order response may be determined, as was described in reference to equation 2 above, where x was determined to be* x_1*, such that the resulting equation can be expressed as* $J(x_1)(x_1-x_0)=b-F(x_0)$*. Note that the approximation of x determined from equation 5 rapidly converges towards the actual solution of F(x)=b assuming that small signals are sufficiently small."* (Gullapalli, paragraphs 0021-0022)].

Bennett, Sanadidi, and Gullapalli are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art to combine the teachings of Bennett and Sanadidi as expressly motivated by Sanadidi in order to "speed up the initial transient phase of a simulation run" (Sanadidi, column 10, lines 6-28). That is, in order to simulate the operating state of an RF circuit, Bennett teaches using an expanded netlist with additional parasitic information (Bennett, column 21, line 52 - column 22, line 19). However,

Bennett also teaches a faster, simpler non-parasitic netlist for simulating the same circuit description (Bennett, column 21, lines 35-52). Sanadidi teaches the "aggregation" or "cloning" simulation technique that would utilize ***both*** Bennett's parasitic model (i.e., "submodel 302" which simulates in "minute detail") and the non-parasitic model (i.e., "submodel 304" which simulates "in simple detail"). Sanadidi further teaches switching from one submodel to the other submodel at certain points during the simulation (Sanadidi, column 17, lines 12-35). The ordinary and predictable result of combining these references would be a simulation with a speedy "initial transient phase" using the "non-parasitic netlist" "simple submodel 304" to initialize the simulation of the RF circuit, and then switching to the "parasitic netlist" "minute detail submodel 302" at the appropriate time in order to accurately simulate the performance of the RF circuit during the operating times with which the user is most concerned. This combination would, in effect, allow a simulation to "fast forward" through simulation times that are not of particular interest using the fast, but less accurate submodel, and switch to the slower, but more accurate submodel during the simulation times that are of particular interest.

Further, it would have been obvious to combine the teachings of Gullapalli with Bennett in view of Sanadidi as expressly motivated by Gullapalli to use a method that *"provide*[s] *for distortion analysis to measure the second and third order deviation of a circuit response from a desired linear response using only first order transfer functions."* (Gullapalli, paragraph 0008). Therefore, a person of ordinary skill would expect to achieve more accurate simulations by combining Gullapalli's teachings with Bennett in view of Sanadidi, and therefore to have higher confidence that the simulation accurately represents the performance of an analog device under design. The ordinary and predictable combination of these references could involve using

Gullapalli's direct solver or linear iterative solver to simulate each circuit description using a system of equations, wherein at least one circuit description corresponds to Bennett's "parasitic netlist" and at least one circuit description corresponds to Bennett's "non-parasitic netlist," while Sanadidi teaches a simulation strategy that uses at least an accurate submodel (i.e. a "parasitic netlist" being represented by a system equations) and a fast submodel (i.e. a "non-parasitic netlist" being represented by a second system of equations) and switching between the at least two submodels in order to produce a single simulation result.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Bennett, Sanadidi, and Gullapalli to arrive at the invention specified in claim 13.

Regarding claim 14, Gullapalli teaches a preconditioner coupled to the linear iterative solver (Gullapalli, paragraphs 0021-0022).

Regarding claim 15, Bennett teaches that the one or more lists include a netlist and a file comprising parasitic information (Bennett, column 21, line 35 - column 22, line 19).

Regarding claim 16, Gullapalli teaches that the simulation kernel evaluates $F(X^i)$, where F is a function and X^i is a value of a varaibel X for an iteration *i*, using the first circuit description and performs a factorization of a Jacobian matrix J built using the second circuit description to solve an equation $J\Delta X = -F(X^i)$ (Gullapalli, paragraphs 0021-0022, et seq.).

Regarding claim 21, Bennett teaches a method of simulating a circuit using an analog or RF simulator (Bennett, column 21, line 35 - column 22, line 19), comprising:

defining two circuit descriptions to be used during the simulation, a first circuit description used for accuracy of the simulation and a second circuit description, different from the first circuit description, used for increasing the speed of the simulation; and simulating the circuit using both the first and second circuit descriptions (Bennett, column 21, line 35 - column 22, line 19); and

outputting the simulation results (Bennett, column 21, line 35 - column 22, line 19).

Sanadidi teaches a simulation system that uses a first submodel ("first circuit description") used for accuracy of the simulation and a second submodel ("second circuit description") used for speed of the simulation, the first submodel being different from the second submodel (Sanadidi, column 17, lines 12-35).

Gullapalli teaches a simulation kernel coupled to the elaboration engine that comprises at least a direct solver or linear iterative solver to simulate the circuit, wherein the simulation kernel solves a system of equations [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations, F(x)=b. The iterative method can be described using the following iterative formula:* [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for j=0 (corresponding to the first iteration), the first order response may be determined, as was described in reference to equation 2 above, where x was determined to be* x_1*, such that the*

resulting equation can be expressed as $J(x_1)(x_1-x_0)=b-F(x_0)$. *Note that the approximation of x determined from equation 5 rapidly converges towards the actual solution of* $F(x)=b$ *assuming that small signals are sufficiently small."* (Gullapalli, paragraphs 0021-0022)].

Bennett, Sanadidi, and Gullapalli are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art to combine the teachings of Bennett and Sanadidi as expressly motivated by Sanadidi in order to "speed up the initial transient phase of a simulation run" (Sanadidi, column 10, lines 6-28). That is, in order to simulate the operating state of an RF circuit, Bennett teaches using an expanded netlist with additional parasitic information (Bennett, column 21, line 52 - column 22, line 19). However, Bennett also teaches a faster, simpler non-parasitic netlist for simulating the same circuit description (Bennett, column 21, lines 35-52). Sanadidi teaches the "aggregation" or "cloning" simulation technique that would utilize ***both*** Bennett's parasitic model (i.e., "submodel 302" which simulates in "minute detail") ***and*** the non-parasitic model (i.e., "submodel 304" which simulates "in simple detail"). Sanadidi further teaches switching from one submodel to the other submodel at certain points during the simulation (Sanadidi, column 17, lines 12-35). The ordinary and predictable result of combining these references would be a simulation with a speedy "initial transient phase" using the "non-parasitic netlist" "simple submodel 304" to initialize the simulation of the RF circuit, and then switching to the "parasitic netlist" "minute detail submodel 302" at the appropriate time in order to accurately simulate the performance of the RF circuit during the operating times with which the user is most concerned. This combination would, in effect, allow a simulation to "fast forward" through simulation times that

are not of particular interest using the fast, but less accurate submodel, and switch to the slower, but more accurate submodel during the simulation times that are of particular interest.

Further, it would have been obvious to combine the teachings of Gullapalli with Bennett in view of Sanadidi as expressly motivated by Gullapalli to use a method that *"provide*[s] *for distortion analysis to measure the second and third order deviation of a circuit response from a desired linear response using only first order transfer functions."* (Gullapalli, paragraph 0008). Therefore, a person of ordinary skill would expect to achieve more accurate simulations by combining Gullapalli's teachings with Bennett in view of Sanadidi, and therefore to have higher confidence that the simulation accurately represents the performance of an analog device under design. The ordinary and predictable combination of these references could involve using Gullapalli's direct solver or linear iterative solver to simulate each circuit description using a system of equations, wherein at least one circuit description corresponds to Bennett's "parasitic netlist" and at least one circuit description corresponds to Bennett's "non-parasitic netlist," while Sanadidi teaches a simulation strategy that uses at least an accurate submodel (i.e. a "parasitic netlist" being represented by a system equations) and a fast submodel (i.e. a "non-parasitic netlist" being represented by a second system of equations) and switching between the at least two submodels in order to produce a single simulation result.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Bennett, Sanadidi, and Gullapalli to arrive at the invention specified in claim 21.

Regarding claim 22, Gullapalli teaches that generating the system of equations comprises solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components, $F(X^i)$ is an evaluated solution, and ΔX is a variable to be solved (Gullapalli, paragraphs 0021-0022, et seq.).

Regarding claim 23, Gullapalli teaches that solving further comprises factorizing the Jacobian matrix J, which is built using the second circuit description, evaluating $F(X^i)$ using the first circuit description, and solving for ΔX (Gullapalli, paragraphs 0021-0022, et seq.).

13. Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bennett in view of Sanadidi as applied to claim 1 above, and further in view of "Transient Analysis" by eCircuit Center ("eCircuit").

Regarding claim 10, neither Bennett nor Sanadidi expressly disclose the existence in the prior art of "any one or more of the following: DC, AC, transient analysis, state-state analysis and modulated steady-state analysis."

eCircuit teaches the existence in the prior art of "any one or more of the following: DC, AC, transient analysis, state-state analysis and modulated steady-state analysis." [*"One of the most complex and intriguing capabilities of the SPICE algorithm is the Transient Analysis."* (eCircuit, "Circuit").

eCircuit and Bennett in view of Sanadidi are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art to combine the teachings of eCircuit with Bennett in view of Sanadidi because Bennett expressly teaches using SPICE to perform circuit simulation (Bennett, column 21, line 35 - column 22, line 19) while eCircuit describes, in greater detail, a feature of SPICE simulation. Further, it would have been obvious to make the combination as expressly motivated by eCircuit in order to "take a collection of resistive and energy-storage components, then find [their] time response to an arbitrary input waveform" (eCircuit, "Circuit"). Therefore, the combination provides greater insight into the performance characteristics of a circuit design, specifically the transient response to an arbitrary input waveform.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Bennett in view of Sanadidi with eCircuit to arrive at the invention specified in claim 10.

14. Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bennett in view of Sanadidi as applied to claim 1 above, and further in view of US Patent No. 6,530,065 to McDonald et al. ("McDonald").

Regarding claim 12, McDonald teaches receiving, on a server computer, a circuit description from a client computer over a distributed network, simulating the description on the server computer, and returning simulation results to the client computer over the distributed network [*"Referring to FIG. 1A, an example of software architecture employed by a server for providing simulation tools is shown as a system 100."* (McDonald, column 5, line 17 et seq.);

"When generating the stored netlists, a developer may employ a block level editor or schematic editor 114 to create such netlists. Examples of schematic editors include Concept from Cadence Design Systems, and Rapid Circuit Development Tool ("RCD") from Transim Technology corporation, as well as others known to those skilled in the relevant art." (McDonald, column 5, lines 60-66)]; *"Under the server system 100, the server initiates a simulation. Using SIMPLIS (which may be forty times faster than PSPICE), waveform simulations are typically completed within two minutes under the simulation control block. Waveform data is then processed under the waveform processing block and downloaded to the user's web browser 101 to be displayed and further processed using a Java-based waveform viewer, described below."* (McDonald, column 6, lines 42-55)].

Bennett in view of Sanadidi and McDonald are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Bennett in view of Sanadidi as expressly motivated by McDonald to provide an online design center that allows end users to quickly select, try and evaluate the manufacturer's products (McDonald, column 4, lines 39-57). Therefore, the combination would enhance the usability of the circuit simulator taught by Bennett in view of Sanadidi.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Bennett in view of Sanadidi to arrive at the invention specified in claim 12.

15. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bennett in view of Sanadidi, further in view of Gullapalli as applied to claim 13 above, and further in view of McDonald.

Regarding claim 17, McDonald teaches a network coupled to the simulator through which the first circuit description is received (McDonald, FIG. 1A, "Internet").

Bennett in view of Sanadidi and Gullapalli and McDonald are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Bennett in view of Sanadidi and Gullapalli as expressly motivated by McDonald to provide an online design center that allows end users to quickly select, try and evaluate the manufacturer's products (McDonald, column 4, lines 39-57). Therefore, the combination would enhance the usability of the circuit simulator taught by Bennett in view of Sanadidi and Gullapalli.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Bennett in view of Sanadidi and Gullapalli to arrive at the invention specified in claim 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jason Proctor/
Primary Examiner, Art Unit 2123

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